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EXAMINER	
PLANTE, JONATHAN R	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,147	HOBSON, LOUIS B.	
	Examiner	Art Unit	
	Jonathan R. Plante	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application Number: 10/812,147 has a total of 24 claims pending in the application; there are 8 independent claims and 16 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

Drawings

3. The drawings are objected to under **37 CFR 1.83(a)** because they fail to text label:

"Figure 2, 200" as "system" (Page 6, Line 3),

"Figure 3, 300" as "system" (Page 8, Line 6),

"Figure 7, 700" as "image forming device" (Page 15, Line 3), and

"Figure 8, 800" as "application programming interface (API)" (Page 16, Line 1) as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. **MPEP § 608.02(d)**. Corrected drawing sheets in compliance with **37 CFR 1.121(d)** are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to **37 CFR 1.121(d)**. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;

(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The abstract of the disclosure is objected to as being unclear and imprecise in disclosing what the applicant is claiming as their invention. Applicant is reminded

> The content of a patent abstract should be such as to enable the reader thereof, regardless of his or her degree of familiarity with patent documents, to determine quickly from a cursory inspection of the nature and gist of the technical disclosure... (MPEP § 608.01(b))

Please replace "**GPIO**" (Line 4) with "GPIO (General Purpose Input Output)" for clarification purposes.

Correction is required. See MPEP § 608.01(b).

The use of the trademarks "Intel Pentium 4", "Pentium", "Microsoft Windows XP", and "Java" have been noted in this application. They should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

The disclosure is objected to because of the following informalities in the specification:

a. Please replace "**illustrate various example**" (Page 1, Line 31) with "illustrate example".

b. Please remove "**so on that illustrate various example**" (Page 1, Line 31).

c. Please remove "**of aspects**" (Page 2, Line 1).

d. Please remove "**various**" (Page 2, Line 28).

e. Please replace "**GPIO**" (Page 6, Line 9) with "GPIO (General Purpose Input Output).

f. Please replace "**0xff**" (Page 7, Line 27) with "0xff (hexadecimal)".

g. Please replace "**used to control establishing**" (Page 7, Line 27) with "used to establish".

h. Please replace "**0x00**" (Page 7, Line 29) with "0x00 (hexadecimal)".

i. Please replace "**used to control establishing**" (Page 7, Line 29) with "used to establish".

j. Please replace "**The memory 604 can store processes**" (Page 14, Line 5) with "The memory 604 can store instructions".

k. Please replace "**systems, methods, and so on have**" (Page 16, Line 25) with "systems and methods".

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claim 1, 9, 10, 11, 12 objected to because of the following informalities:

a. Please replace "**may be**" (Claim 1, Line 3) with "are".

b. Please replace "**GPIO block and**" (Claim 1, Line 4) with "GPIO block(s) and".

c. Please replace "**GPIO block is**" (Claim 1, Line 4) with "GPIO block(s) or the thermal management register are".

d. Please replace "**that can be**" (Claim 1, Line 5) with "that is".

e. Please replace "**to select a**" (Claim 1, Line 7) with "the logic selecting a".

f. Please remove "**to be written to the GPIO block or the thermal management register**" (Claim 1, Line 7).

g. Please replace "**GPIO block or**" (Claim 1, Line 9) with "GPIO block(s) or".

h. Please replace "**may be**" (Claim 9, Line 4) with "are".

i. Please replace "**GPIO block and**" (Claim 9, Line 5) with "GPIO block(s) and".

j. Please replace "**GPIO block is**" (Claim 9, Line 5) with "GPIO block(s) or the thermal management register are".

k. Please replace "**that can be**" (Claim 9, Line 6) with "that is".

l. Please replace "**to select a**" (Claim 9, Line 8) with "the logic selecting a".

m. Please remove "**to be written to the GPIO block or the thermal management register**" (Claim 9, Line).

n. Please replace "**GPIO block or**" (Claim 9, Line 10) with "GPIO block(s) or".

o. Please replace "**may be**" (Claim 10, Line 4) with "are".

p. Please replace "**GPIO block and**" (Claim 10, Line 5) with "GPIO block(s)

and".

q. Please replace "**GPIO block is**" (Claim 10, Line 5) with "GPIO block(s) or the thermal management register are".

r. Please replace "**that can be**" (Claim 10, Line 6) with "that is".

s. Please replace "**to select a**" (Claim 10, Line 8) with "the logic selecting a".

t. Please remove "**to be written to the GPIO block or the thermal management register**" (Claim 10, Line).

u. Please replace "**GPIO block or**" (Claim 10, Line 10) with "GPIO block(s) or".

v. Please replace "**its**" (Claim 11, Line 3) with "the processor".

w. Please replace " **the processor one of, the actual thermal management signal and the simulated thermal management signal**" (Claim 11, Line 6) with "the processor only the actual thermal management signal or the simulated thermal management signal but not both". This change is requested to clarify the language of the claim and to conform to applicants definition and language provided for in the application for the usage of the "exclusive or" logic operand (Page 17, Line 9).

x. Please replace "**may be**" (Claim 12, Line 3) with "are".

y. Please replace "**GPIO block and**" (Claim 12, Line 4) with "GPIO block(s) and".

z. Please replace "**GPIO block is**" (Claim 12, Line 4) with "GPIO block(s) or the thermal management register are".

aa. Please replace "**that can be**" (Claim 12, Line 5) with "that is".

bb. Please replace "**to select a**" (Claim 12, Line 7) with "the logic selecting a".

cc. Please remove "**to be written to the GPIO block or the thermal management register**" (Claim 12, Line 7).

dd. Please replace "**GPIO block or**" (Claim 12, Line 9) with "GPIO block(s) or".

ee. Please remove "**the state of**" (Claim 14, Line 3).

ff. Please replace "**a**" (Claim 14, Line 6) with "the".

gg. Please replace "**can be**" (Claim 18, Line 2) with "are".

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-13, and 23 are rejected as a result of the applications disclosure pertaining to the provided definition of "Logic" (Page 3, Line 29) the application defines "logic" as:

> Includes but is not limited to hardware, **firmware**, **software** and /or combinations of each to perform a function(s) or an action(s), and/or to cause a function or action from another logic, method, and/or system. For example, based on a desired application or needs, logic may include a **software** controlled microprocessor, discrete logic like an application specific integrated circuit (ASIC), a programmed logic device, a memory device containing instructions, or the like. Logic may include one or more gates, combinations of gates, or other circuit components. Logic may also be **fully embodied as software**. (Page 3, Line 29 – Page 4, Line 4)

As a result of the "logic" being considered the fundamental invention or improvement of prior art in the application "logic" under 35 U.S.C. 101 constituting of firmware and/or software code lack the necessary physical articles or objects to constitute a machine or

a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within the statutory category. They are, at best, functional descriptive material *per se*. As a result of applicant defining "logic" as being inclusive of these non-statutory items results in "logic" being considered non-statutory subject matter.

Claims 22 and 24 are rejected as a result of the applications disclosure pertaining to the provided definition of a "computer-readable medium" (Page 3, Line 9) the application defines a "computer-readable medium" as:

> a medium that participates in directly or indirectly providing **signals**, instructions and/or data. A computer-readable medium may take the forms, including but limited to, non-volatile medium, volatile media, and transmission media. Non-volatile media may include, for example, optical or magnetic disks, dynamic memory and the like. Transmission media may include coaxial cables, copper wire, fiber optic cables, and the like. Transmission media can also take the form of **electromagnetic radiation**, like that generated during **radio-wave** and **infra-red** data communications, or take the form of one or more groups of **signals**. Common forms of computer-readable medium include, but are not limited to, a floppy disk, a flexible disk, a hard disk, a magnetic tape, other magnetic medium, a CD-ROM, other optical medium, punch cards, paper tape, other physical medium with patterns and holes, a RAM, a ROM, an EPROM, a FLASH-EPROM, or other memory chip or card, a memory stick, a **carrier wave/pulse**, and other media from which a computer, a processor or other electronic device can read. **Signals** used to propagate instructions or other software over a network, like the Internet, can be considered a "computer-readable medium." (Page 3, Lines 9-24)

Under 35 U.S.C. 101 signals, electromagnetic radiation, radio waves, infrared radiation, and carrier waves/pulses lack the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within the statutory

category. They are, at best, functional descriptive material *per se*. As a result of applicant defining "computer-readable medium" as being inclusive of these non-statutory items results in "computer-readable medium" being considered non-statutory subject matter.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-24 contain reference to simulate/simulation (**Simulate**: to give or create the effect or appearance of. / **Simulation**: the imitation by one system or process of the way in which another system or process works. (The Merriam-Webster Dictionary, 2005)).

The specification is silent on how one skilled in the art would conduct or produce a simulation of claimed system. The specification fails to disclose details pertaining to and not limited to a model of the system, means for measuring the system, a system for performing calculations, a system for generating a simulation, and a process of generating a simulation.

Applicant is requested to specifically cite (reference) support in the specification for claims 1-24 in reference to the simulation claims in response to this office action without the addition of new subject matter.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "**based on the thermal management signal**" (Line 3). There is insufficient antecedent basis for this limitation in the claim. For purpose of examination it will be interpreted that the applicant is referring to an additional thermal management signal that carries the signal to the processor or that is contained in the processor. Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. (US Patent 6,535,798 B1 (March 18, 2003)).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to acknowledge that the system claimed in Bhatia et al. leads also to the development of a model or simulation of that system.

The motivation for doing so would have been the development of a model or simulation during the research and development (R&D) phase of an 80x86 or Pentium® family processor from Intel Corporation that implemented the system claimed in Bhatia et al. and that also conforms to the Advanced Configuration and Power Interface (ACPI) Specification (Rev. 1.0, published on December 22, 1996). During the research and development (R&D) phase of the Pentium® family it would be obvious to one trained in the art that the Intel Corporation (Assignee of Bhatia et al.) would generate high level logic (i.e. VHDL or VERILOG) models of the Pentium® family processors in addition to timing (frequency) and power models.

For purpose of examining claims 1-24 applicant is reminded that they have defined the following terms as being inclusive of the following:

> "Data store", as used herein, refers to a physical and/or logical entity that can store data. A data store may be, for example, a database, a table, a file, a list, a queue, a heap, a memory, a register, and so on. A data store may reside in one logical and/or physical entity and/or may be distributed between two or more logical and/or physical entities. (Page 3, Line 25)

> "Logic", as used herein, includes but is not limited to hardware, firmware, software and/or combinations of each to perform a function(s) or an action(s), and/or to cause a function or action from another logic, method, and/or system. For example, based on a desired application of needs, logic may include a software controlled microprocessor, discrete, logic like an application specific integrated circuit (ASIC), a programmed logic device, a memory device containing instructions, or the like. Logic may include one or more gates, combinations of gates, or other circuit components. Logic may also be fully embodied as software. Where multiple logical logics are described, it may be possible to incorporate the multiple logical logics into one physical logic. Similarly, where a single logical logic is described, it may be possible to distribute that single logical logic between multiple physical logics. (Page 3, Line 29)

As a result the examination of claims 1-24 will be interpreted in reference to the above definitions in the broadest terms relative to location(s) of structure(s), but the structure(s) will be examined as maintaining their functionality of the "data store" and "logic" as defined.

As per claim 1, Bhatia et al. discloses, "a processor performance state in a processor, **[a thermal management controller that may include one or more layers including software, firmware, and hardware. Example components may include general or special-purpose processors such as microprocessors, microcontrollers, application-specific integrated circuits (ASICs), programmable gate arrays (PGAs), peripheral devices controllers, and other types of devices. In one embodiment, one low performance state is defined along with a high performance, and optionally, one or more intermediate performance states. (Column 2, Line 29)]** "comprising: a data structure stored in a memory, the data structure being configured to store an address of a GPIO block" **[the interrupt event may be stored as a memory or I/O mapped register (Column 4, Line 5)]** "and a set of bit patterns that may be written to one or more of, the GPIO block and a thermal management register in the processor, where the GPIO block is configured to control a thermal management signal that can be provided to the processor" **[the power management module indicates a new performance state of the processor is to transition to. This may be performed, for example, by writing a predefined value to a control register to indicate the new performance state of the processor. The**

control register may be defined in the memory or I/O address space (Column 12, Line 39)] "a logic operably connected to the memory, the logic configured to receive a request to establish a desired processor performance state in the processor" **[power management control logic according to an embodiment of the invention for controlling the core clock frequency and the supply voltage level of the processor (Column 10, Line 41)]** "to select a bit pattern to be written to the GPIO block or the thermal management register, the bit pattern being selected from a set of bit patterns, and to write the bit pattern to the GPIO block or the thermal management register" **[The control register is accessible by hardware control logic (which may be implemented in the host bridge 18, for example) to control activation and deactivation of the processor's clock control input (e.g., G_STPCLK#). The number of register bits dedicated to store the clock duty cycle setting determines the number of different duty cycle settings that may be made by the hardware control logic. (Column 9, Line 19)]** "where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state." **[In the HP state, a processor's (or other component's) core clock frequency and voltage level may be at one setting, while in the LP state, the processor's core clock frequency and voltage level may be at a lower setting. (Column 2, Line 45)]**.

As per claim 2, Bhatia et al. discloses, "where the data structure is further configured to store an address of an ACPI status register from which a value related to a frequency and a voltage established in the processor can be read" **[Detection of**

whether the processor 12 is in the HP or LP state may be accomplished by reading predefined registers in the processor 12 or in other components in the system, including the voltage regulator 52 or the system memory 16. (Column 7, Line 13)].

As per claim 3, Bhatia et al. discloses, "where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." **[Various software or firmware layers (formed of modules or routines, for example), including applications, operating systems modules, device drivers, BIOS modules, and interrupt handlers, may be stored in one or more storage media in the system. The storage media includes the hard disk drive, CD or DVD drive, floppy drive, non-volatile memory, and system memory. (Column 5, Line 3)]**.

As per claim 4 Bhatia et al. discloses, "where the data structure comprises an ACPI table stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processors function. **[Referring to FIG. 3, according to an alternative embodiment, the thermal management routine may be implemented in another software layer (e.g., an OS module, device driver, BIOS routine). In one example, the thermal management routine invoked may be in response to an ACPI event (e.g., thermal management SCI), which causes the OS to perform thermal mnagement task. Thus, the thermal management routine in this example may be under control of the OS. (Column 7, Line 57)]**

As per claim 5, Bhatia et al. discloses, "where the data structure comprises an ACPI table stored in a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." **["Advanced Configuration and Power Interface (ACPI) Specification, Rev. 1.0, published on Dec. 22, 1996, that provides an interface between the operating system of a system and hardware devices to implement power and thermal management" (Column 1, Line 13)** and combining **"Referring to FIG. 3, according to an alternative embodiment, the thermal management routine may be implemented in another software layer (e.g., an OS module, device driver, BIOS routine)." (Column 7, Line 57)]**. Bhatia et al. teaches both the usage of the ACPI Specification and the BIOS in the system and it would be obvious to one skilled in the art that the BIOS could store the instructions/table of the ACPI Specifications. Applicant is further reminded of the definitions for "Data store" and "Logic" discussed above and in the application disclosure.

As per claim 6, Bhatia et al. discloses, "where the set of bit patterns facilitates two processor performance states that correspond to a higher performance state and a lower performance state." **[A clock duty cycle setting representing the current performance level P_n may be written by a thermal management module (implemented as in interrupt handler, BIOS routine, or device driver, as examples) to control the register (which may be located in the processor or other suitable storage location) to define the percentage of maximum performance desired of the processor 12 (in other words, to define how much processor clock throttling should be performed). The control register is accessible by hardware control**

logic (which may be implemented in the host bridge 18, for example) to control activation and deactivation of the processor's clock control input (e.g., G_STPCLK#). The number of register bits dedicated to store the clock duty cycle setting determines the number of different duty cycle settings that may be made by the hardware control logic. (Column 9, Line 12)].

As per claim 7, Bhatia et al. discloses, "where the thermal management register comprises the TM2 register in a Pentium microprocessor" **[A clock duty cycle setting representing the current performance level P_n may be written by a thermal management module (implemented as in interrupt handler, BIOS routine, or device driver, as examples) to control the register (which may be located in the processor or other suitable storage location) (Column 9, Line 12)].** Bhatia et al. teaches the usage of a delegated register to facilitate the thermal management of the processor and to one skilled in the art it would be obvious to associate a Pentium microprocessor in generic terms as a processor.

As per claim 8, Bhatia et al. discloses, "where the thermal management signal comprises a signal placed on the PROCHOT line available to a Pentium microprocessor" **[To perform throttling, a clock control input (such as the stop clock input illustrated as G_STPCLK# in FIG.1 to an 80x86 or Pentium® family processor from Intel Corporation) (Column 4, Line 8)].** Bhatia et al. teaches the usage of a control signal to a Pentium® family processor and to one skilled in the art it would be obvious that the **G_STPCLK#** and **PORCHOT** signals are equivalent in performing the same function of transmitting a control signal to the processor.

As per claim 9, please see rejection to claim 1. In addition to one skilled in the art it would be obvious that "A system" (Claim 1, Line 1) and "A computer configured with a system" (Claim 9, Line 1) are equivalent systems and perform the equivalent function.

As per claim 10, please see rejection to claim 1. In addition to one skilled in the art it would be obvious that "A system" (Claim 1, Line 1) and "A printer configured with a system" (Claim 9, Line 1) are equivalent systems and perform the equivalent function.

As per claim 11, Bhatia et al. discloses, "simulating a processor performance state in a processor that is configured to receive an actual thermal management signal from a thermal management circuit and to selectively change its operating frequency based on the thermal management signal," **["a thermal management scheme in which one or more systems components are switched between different levels (two or more) of performance states in response to a over-temperature conditions or other conditions" (Column 2, Line 24)** and **"In the HP state, a processor's (or other component's) core clock frequency and voltage level may be at one setting, while in the LP state, the processor's core clock frequency and voltage level may be at a lower setting" (Column 2, Line 45)]** "the system comprising: a simulation logic configured to produce a simulated thermal management signal;" **["The thermal management scheme is performed by a thermal management controller that may include one or more layers including software, firmware, and hardware" (Column 2, Line 28)** and **"The signal G_STPCLK# is generated by the thermal management control logic and is routed to the STP_CLK# input pin of the processor (Column**

4, Line 12)] "a combination logic configured to selectively provide to the processor one of, **[a thermal management controller that may include one or more layers including software, firmware, and hardware (Column 2, Line 29)** the actual thermal management signal **[One or more temperature senor units 15 monitor system temperature in one or more corresponding thermal zones, each capable of issuing an interrupt, e.g., a system management interrupt (SMI), a system controller interrupt (SCI), or some other notification when a sensed temperature rises above a preset target temperature T_t or falls below the target temperature T_t. (Column 3, Line 33)** and the simulated thermal management signal." **["The thermal management scheme is performed by a thermal management controller that may include one or more layers including software, firmware, and hardware" (Column 2, Line 28)** and **"the thermal management may be performed in an ACPI environment" (Column 3, Line 15)]**.

As per claim 12, please see rejection to claim 1. In addition to applicant is further reminded of the definition of "Logic" discussed above and in the application disclosure.

As per claim 13, please see rejection to claim 7. Additionally, it would be obvious to one trained in the art that a "Pentium 4" microprocessor is a corporation trademark/marketing term equivalent to the term "a processor" in generic language.

As per claim 14, please see rejection to claim 1. Claim 14 is broader in scope than claim 1 and as a result is rejected on the basis that claim 1 has been rejected.

As per claim 15, please see rejection to claim 5. It is obvious to one skilled in the art that "data structure comprises an ACPI table stored" (claim 5) and "establishing a data structure as an ACPI table" (claim 15) is equivalent language/terms.

As per claim 16, Bhatia et al. discloses, "where establishing the data structure includes writing a set of bit patterns to the ACPI table and writing the address to the GPIO block to the ACPI table. **["A clock duty cycle setting representing the current performance level P_n may be written by a thermal management module (implemented as in interrupt handler, BIOS routine, or device driver, as examples) to control the register (which may be located in the processor or other suitable storage location) to define the percentage of maximum performance desired of the processor 12 (in other words, to define how much processor clock throttling should be performed). The control register is accessible by hardware control logic (which may be implemented in the host bridge 18, for example) to control activation and deactivation of the processor's clock control input (e.g., G_STPCLK#). The number of register bits dedicated to store the clock duty cycle setting determines the number of different duty cycle settings that may be made by the hardware control logic." (Column 9, Line 12)** and **"the thermal management may be performed in an ACPI environment" (Column 3, Line 15)].** Bhatia teaches the usage of the ACPI Specification and environment and also the usage of a "control register that is accessible by hardware" (understood to one skilled in the art that a register can be considered a set of latches, a GPIO, or a delegated partition or sub-partition of memory such as system memory, hard drive, or BIOS) and

that the hardware would access the data via a memory pointer or address stored in the register.

As per claim 17, please see rejection to claim 6.

As per claim 18, Bhatia et al. discloses, "where the simulation data comprises a set of bit patterns" **[The control register is accessible by hardware control logic (which may be implemented in the host bridge 18, for example) to control activation and deactivation of the processor's clock control input (e.g., G_STPCLK#). The number of register bits dedicated to store the clock duty cycle setting determines the number of different duty cycle settings that may be made by the hardware control logic. (Column 9, Line 19)]** "that can be written to one or more of, the thermal management registers, and the GPIO block" **[the interrupt event may be stored as a memory or I/O mapped register (Column 4, Line 5)]**.

As per claim 19 please see response to claim 7.

As per claim 20 please see response to claim 8.

As per claim 21, Bhatia et al. discloses, "acquiring an address of an ACPI status register configured to report a value related to the operating frequency and the operating voltage of the processor;" **[Detection of whether the processor 12 is in the HP or LP state may be accomplished by reading predefined registers in the processor 12 or in other components in the system, including the voltage regulator 52 or the system memory 16. (Column 7, Line 13)]** "reading the value from the ACPI status register; and selectively reporting a success or error condition based on the value." **["The thermal management routine, according to the alternative**

embodiment, periodically samples the system temperature (T_n) from the temperature sensor 15, which may contain a memory- or I/O-mapped register value accessible by the system software or firmware to poll the sensed temperature." (Column 7, Line 66) and **"Next the routine waits (at 309) a predetermined time period before comparing the next sampled temperature T_n to the target temperature T_t. If T_n is less then Tt, then the processor is transitioned bak to the HP state" (Column 8, Line 14)].** Bhatia teaches the detection of the processor status and also the comparison or the status value to a predetermined value. It is obvious to one skilled in the art that a detection for an error (over heating) and the comparison of sampled temperature value to the predetermine temperature value are equivalent functions and serve the same function of confirming that the processor is not over-heating.

As per claim 22, please see rejection to claim 1. Claim 22 is broader in scope than claim 1 and as a result is rejected on the basis that claim 1 has been rejected.

As per claim 23, please see rejection to claim 1. Claim 23 is broader in scope than claim 1 and as a result is rejected on the basis that claim 1 has been rejected.

As per claim 24, Bhatia et al. discloses, "A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a processor performance state in a processor by controlling a thermal management signal, comprising: a first interface for communicating a bit pattern data; a second interface for communicating a GPIO block address data; and a third interface for communicating a state data, where the state data is related to a

simulated processor performance state generated by applying the bit pattern to a GPIO block identified by the GPIO block address data." [**In addition, instead of being configured with host and system bridges 18 and 34 as illustrated in FIG. 1, the circuitry may be implemented as a memory hub (including interfaces to the processor and system memory) and an input/output (I/O) hub (including interfaces to the system bus and secondary bus). In this other configuration, the control logic 100, 102 may be implemented in the memory hub. With the memory and I/O hubs, messages rather than signals may be used to provide the same functionality as the control logic 100, 102. (Column 10, Line 53)**].

Conclusion

11. In addition to reference used under 35 U.S.C. 102, additional prior art references that disclose relevant subject matter on the merits can be found in SYSTEM AND METHOD FOR MANAGING A PLURALITY OF PROCESSOR PERFORMANCE STATES, Cooper US 6,457,135 (September 24, 2002) and INDEPENDENTLY CONTROLLING PASSIVE AND ACTIVE COOLING IN A COMPUTER SYSTEM, Peters et al. US 6,470,289 (October 22, 2002).

Cooper:

a. Processor capable of operating at a plurality of performance states. (abstract)

b. Temperature below passive threshold. (FIG. 6)

c. Application of the ACPI Specification (Column 1, Line 48)

d. Low power state / High performance state (Column 5, Line 40)

e. Software communicates with hardware/BIOS (Column 6, Line 2)

f. Throttling (Column 15, Line 12)

g. Usage of registers (Column 15, Line 33)

h. Voltage and frequency (Column 16, Line 67)

Peters et al.

a. Thermal control logic that efficiently cools the computer (abstract)

b. Temperature senor (FIG. 1)

c. Register bits (FIG. 3)

12. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

13. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571)

272-9780. The examiner can normally be reached on Monday through Friday 9:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pierre M. Vital can be reached on (571) 272-4215. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 26, 2006
JRP

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